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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,745	04/02/2004	Chang-fen Hu	TSMC2003-0988(N1280-00170	1384

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EXAMINER	
HOANG, ANN THI	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 02/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/816,745	HU, CHANG-FEN	
	Examiner	Art Unit	
	Ann T. Hoang	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *02 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 300, 400. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 6, 12 and 15 are objected to because the limitation of "a thickness of a gate oxide for a regular transistor of the IC, not for using as a capacitor" is not supported by the disclosure. The disclosure appears to discuss only the thickness of a gate oxide for a transistor used as a capacitor on page 6, lines 18-23. There is no mention of thickness of a gate oxide for a transistor not used as a capacitor. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4, 6-10, and 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 6,392,860) in view of Andresen et al. (US 6,310,379) and Shau (US 6,343,045).

Regarding claim 1, Lin et al. discloses an electro-static discharge protection circuit (20) for an integrated circuit comprising: an RC module (28, 30) having a resistor (28) and capacitor (30) connected in series; and a current dissipation module (22) for dissipating the ESD. See Fig. 2. Lin et al. does not disclose that capacitor (30) is formed by a thick native gate oxide of a transistor.

However, Andresen et al. discloses a capacitor (N4), formed by a thick gate oxide of a transistor, as part of an RC module (R2, N4) in an ESD protection circuit (120). Capacitor (N4) triggers current dissipation module (N2) during an ESD event occurring at a pad (113) so that the ESD can be diverted to ground. See Fig. 2 and column 6, lines 40-53. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the capacitor formed by a thick gate oxide of a transistor of Andresen et al. in the ESD protection circuit of Lin et al. in order to provide an inexpensive and durable capacitor, since capacitors formed at the gate of transistors typically have a long life span due to effective temperature control and are inexpensive due to their simplicity. The reference does not disclose that the thick gate oxide of the transistor forming the capacitor (N4) is formed as a native device.

However, Shau discloses using the gate oxide of a transistor (1700) as a capacitor and forming transistor (1700) as a native device in order to prevent leakage current therethrough. See Fig. 23A and column 27, lines 9-20. It would have been obvious to one of ordinary skill in the art at the time of the invention to form the thick gate oxide of the transistor of Andresen et al. as a native device, as disclosed by Shau, in order to prevent leakage current through the thick gate oxide of the transistor. A capacitor formed by a thick native gate oxide of a transistor would not only prevent leakage current therethrough; it would also keep the input (B) of current dissipation module (22) low and prevent current dissipation module (22) of Lin et al. from entering a driven state, thus avoiding leakage current through the current dissipation module (22) during a normal operation of the IC.

Regarding claim 2, Lin et al. discloses that current dissipation module (22) is an NMOS transistor connected between a power line (Vdd) of the IC and a grounding line (Vss) of the IC. See Fig. 2 and column 2, lines 2-3. Fig. 2 does not show a pad connected to current dissipation module (22). However, Lin et al. discloses in column 1, lines 25-27 that ESD protection circuit (20) is connected to a pad of the IC, therefore it is understood that a pad would be connected to ESD protection circuit (20) at the power terminal (Vdd), making the current dissipation module (22) connected between a pad of the IC and a grounding line (Vss) of the IC.

Regarding claim 3, Lin et al. discloses a control module (24, 26) connected between the RC module and the current dissipation module (22) for controlling the current dissipation module (22). See Fig. 2 and column 2, lines 24-29.

Regarding claim 4, Lin et al. shows in Fig. 2 that control module (24, 26) is an inverter.

Regarding claim 7, the transistor forming a capacitor, as provided by the combination of Lin et al. in view of Andresen et al. and Shau in above claim 1, would have a threshold voltage close to zero because of its thick native gate oxide.

Regarding claim 8, Lin et al. discloses an ESD protection circuit (20) for an IC comprising: an RC module (28, 30) having a resistor (28) and capacitor (30) connected in series; a control module (24, 26) coupled to the RC module (28, 30); and a current dissipation module (22) controlled by the control module (24, 26) for dissipating the ESD. See Fig. 2. Lin et al. does not disclose that capacitor (30) is formed by a thick native gate oxide of a transistor.

However, Andresen et al. discloses a capacitor (N4), formed by a thick gate oxide of a transistor, as part of an RC module (R2, N4) in an ESD protection circuit (120). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the capacitor formed by a thick gate oxide of a transistor of Andresen et al. in the ESD protection circuit of Lin et al. in order to provide an inexpensive and durable capacitor. See corresponding rejection on claim 1. The reference does not disclose that the thick gate oxide of the transistor forming the capacitor (N4) is formed as a native device.

However, Shau discloses using the gate oxide of a transistor (1700) as a capacitor and forming transistor (1700) as a native device in order to prevent leakage current therethrough. It would have been obvious to one of ordinary skill in the art at the time of the invention to form the thick gate oxide of the transistor of Andresen et al. as a native device, as disclosed by Shau, in order to prevent leakage current through the thick gate oxide of the transistor. The transistor forming a capacitor, as provided by the above combination, would have a threshold voltage close to zero because of its thick native gate oxide. A capacitor formed by a thick native gate oxide of a transistor would also avoid leakage current through the current dissipation module (22) of Lin et al. during a normal operation of the IC. See corresponding rejection on claim 1.

Regarding claim 9, claim 9 corresponds to claim 2 and is rejected under the same reasoning as that of claim 2. See above rejection.

Regarding claim 10, claim 10 corresponds to claim 4 and is rejected under the same reasoning as that of claim 4. See above rejection.

Regarding claim 13, Lin et al. discloses an ESD protection circuit (20) for an IC comprising: an RC module (28, 30) having a resistor (28) and capacitor (30) connected in series; an inverter module (24, 26) with its input coupled to a connection point (A) between the resistor (28) and the capacitor (30); and a current dissipation module (22) for dissipating the ESD having one transistor (22) with an output (B) of the inverter (24, 26) controlling the gate thereof. See Fig. 2. Lin et al. does not disclose that capacitor (30) is formed by a thick native gate oxide of a transistor.

However, Andresen et al. discloses a capacitor (N4), formed by a thick gate oxide of a transistor, as part of an RC module (R2, N4) in an ESD protection circuit (120). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the capacitor formed by a thick gate oxide of a transistor of Andresen et al. in the ESD protection circuit of Lin et al. in order to provide an inexpensive and durable capacitor. See corresponding rejection on claim 1. The reference does not disclose that the thick gate oxide of the transistor forming the capacitor (N4) is formed as a native device.

However, Shau discloses using the gate oxide of a transistor (1700) as a capacitor and forming transistor (1700) as a native device in order to prevent leakage current therethrough. It would have been obvious to one of ordinary skill in the art at the time of the invention to form the thick gate oxide of the transistor of Andresen et al. as a native device, as disclosed by Shau, in order to prevent leakage current through the thick gate oxide of the transistor. The transistor forming a capacitor, as provided by the above combination, would have a threshold voltage close to zero because of its thick

native gate oxide. A capacitor formed by a thick native gate oxide of a transistor would also avoid leakage current through the current dissipation module (22) of Lin et al. during a normal operation of the IC. See corresponding rejection on claim 1.

Regarding claim 14, claim 14 corresponds to claim 2 and is rejected under the same reasoning as that of claim 2. See above rejection.

Regarding claims 6, 12 and 15, the references disclose the claimed invention except that the thickness of a gate oxide for a regular transistor of the IC, not for using as a capacitor, is below 60 Angstroms. It would have been obvious to one of ordinary skill in the art at the time of the invention to determine the best range of gate oxide thickness for the transistors, since it has been held that, where the general conditions of a claim are discloses in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

6. Claims 5 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 6,392,860) in view of Andresen et al. (US 6,310,379) and Shau (US 6,343,045), as applied to claims 3 and 8 above, and further in view of Chen et al. (US 2003/0223166). Regarding both claims 5 and 11, none of the references applied above disclose a control module consisting of a signal NMOS transistor.

However, Chen et al. discloses an ESD protection circuit (12) comprising a control module (Mn2) that is an NMOS transistor. The NMOS transistor is connected to an RC module (R2, C2) and controls the turning on of current dissipation modules (Mp21, Mp22, Mp2). See Fig. 4 and page 4, paragraph 55. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the control module

consisting of an NMOS transistor of Chen et al. in the ESD protection circuit of Lin et al. in order to reduce the number of components and space needed for the control module.

7. Claims 6, 12 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 6,392,860) in view of Andresen et al. (US 6,310,379) and Shau (US 6,343,045), as applied to claims 1, 8 and 13 above, and further in view of Ramappa (US 6,812,050). Regarding claims 1, 8 and 13, none of the references applied above disclose that a thickness of a gate oxide for regular transistor of the IC, not for using as a capacitor, is below 60 angstroms.

However, Ramappa discloses that, due to the scaling of present day transistor devices for ICs, these transistors typically have a gate oxide thickness of 12-24 Angstroms. Ramappa is referring to regular transistors of ICs, not for using as a capacitor. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the gate oxide thickness below 60 Angstroms, as disclosed by Ramappa, for the regular transistors of the ESD protection circuit of Lin et al. in order to scale down the non-capacitor devices of the IC in order to reduce the size of the IC.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ker et al. (US 2002/0130390) discloses ESD protection circuit with an RC module in which the capacitor is formed by a gate oxide of a transistor, an inverter, and a current dissipation module (see Fig. 6). Lin et al. (US 2002/0153570) discloses an ESD protection circuit that uses a native NMOS as a current dissipation

module in order to have a quicker trigger-on rate. Metz et al. (US 5,452,171) and Lee (US 5,565,790) both disclose an ESD protection circuit in which a control module for controlling a current dissipation module is an NMOS transistor. Chang et al. (US 4,144,634) discloses the use of a thick native gate oxide of a transistor as a charge storage device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ann T. Hoang, whose telephone number is 571-272-2724. The examiner can normally be reached Monday through Friday, 8:00 a.m. to 5:00 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus, can be reached at 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ATH
1/26/06

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